METHODS OF FORMING SELF-ALIGNED CONTACT STRUCTURES IN SEMICONDUCTOR INTEGRATED CIRCUIT DEVICES

Abstract of the Disclosure

Methods of forming integrated circuit devices (e.g., memory devices) include the use of preferred self-aligned contact hole fabrication steps. These steps improve process reliability by reducing the likelihood that contact holes will become misaligned to underlying integrated circuit device structures and thereby potentially expose the structures in an adverse manner. Typical methods include the steps of forming a plurality of interconnection patterns on a substrate and then covering a surface of the interconnection patterns and a portion of the substrate with a capping insulating layer such as silicon nitride layer. The capping insulating layer is then covered with an upper interlayer insulating layer different from the capping insulating layer. The upper interlayer insulating layer and the capping insulating layer are then dry-etched in sequence to form a first narrow contact hole that exposes the substrate, but preferably does not expose the interconnection patterns. The first contact hole is then widened in a self-aligned manner using the capping insulating layer as an etch-stop layer. This widening step is performed by wet etching sidewalls of the first contact hole using an etchant that etches the upper interlayer insulating layer faster than the capping insulating layer. In this manner, the first contact hole may be formed to initially compensate for potential misalignment errors and then a self-aligned wet etching step may be performed to widen the first contact hole into a second contact hole so that low resistance contacts (e.g., contact plugs) can be provided therein.